University of California, Santa Barbara

Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

Midterm Exam #2
November 16, 2006

Name _____

Perm # _____

Lab Section _____

Problem #1 (25 points) _____

Problem #2 (25 points) _____

Problem #3 (25 points) _____

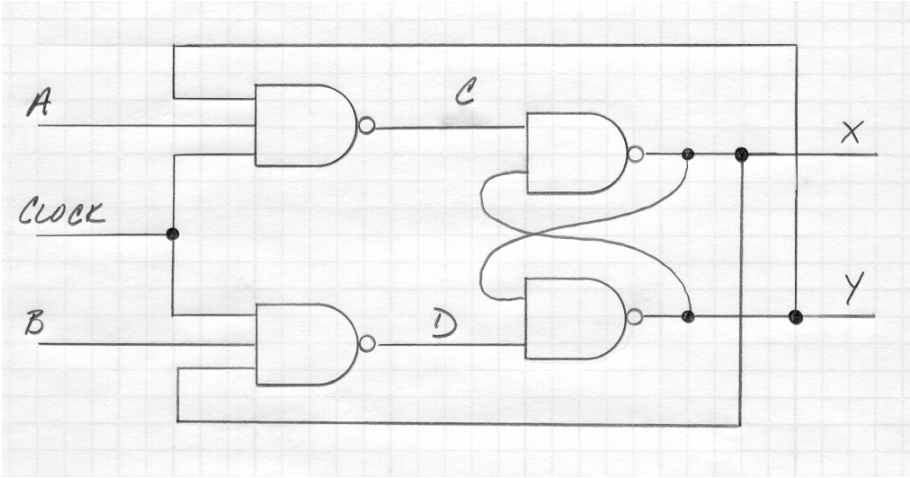
Problem #4 (25 points) _____

Total (100 points) _____

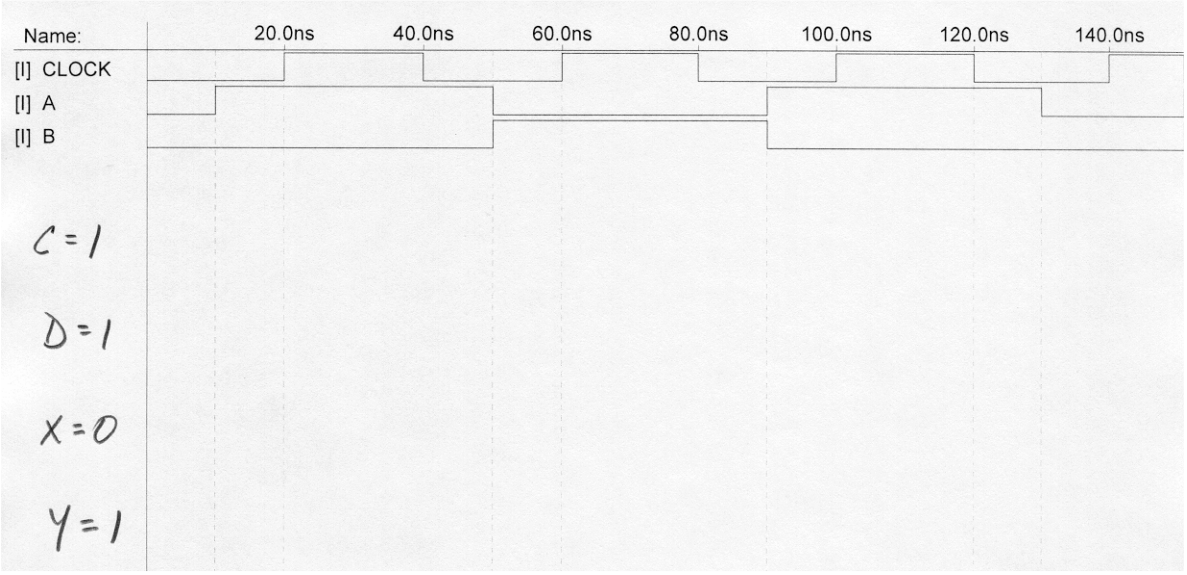
- This is a 75 minute exam; closed book, closed notes, no calculators.
- Answer all questions (except timing diagrams) on the paper provided by the instructor; answer timing diagram problems on exam sheet.
- Write on only one side of the paper.
- Attach answer sheets to this exam in the correct order.
- Include your name and perm # on every sheet.

Problem #1.

Complete the timing diagram for the gated latch shown below. Use arrows to indicate the sequence of signal transitions. Assume the gate delays are much shorter than the clock period.



Initial conditions as shown on the timing diagram: C = D = 1, X = 0 and Y = 1.



Problem #2.

In this problem you are to design a two-bit counter (state variables A and B). The counter has a two-bit input, x and y. When xy = 01 the counter is incremented by one and when xy = 10 the counter is incremented by 2; with xy = 00 the count remains the same and with xy = 11, the count is reset to 00.

1. Construct both a state table and a state diagram for the counter.

2. Construct the next state maps for the A and B state variables and determine next equations (A^+ , B^+).

3. If this counter were implemented with D flip flops, what would the D inputs to the A and B flip flops be?

4. Using the template below, provide the Verilog code to implement the counter. (Don't worry about initializing the counter; you can assume the initial state is zero).

```
module mid2counter (clock, x, y, A, B);

input clock, x, y;
output A, B;
reg [1:0] state;

parameter [1:0] zero = 2'b00, one = 2'b01, two = 2'b10, three = 2'b11;

assign {A,B} = state;

always @ (posedge clock)
        begin

***Insert Verilog code here***

        end
endmodule
```

Problem #3.

A finite state machine is constructed using positive edge triggered, T flip flops.

The input equations for the two T flip flops are:

$$T_A = x + B'$$
$$T_B = A' + B$$

The output equation for the machine is:

$$z = xA' + x'A$$

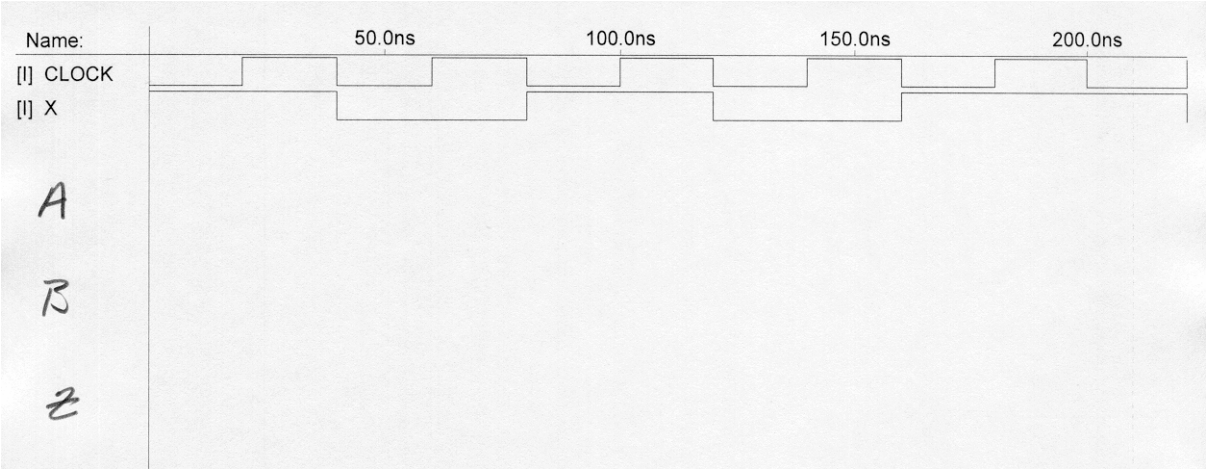
1. Derive next state equations for the flip flops (recall the characteristic equation for a T flip flop is Q+ = T XOR Q = TQ' + T'Q).

2. Map the next state equations and output function on K maps.

3. Construct a state table for the machine.

4. Construct a state diagram for the machine.

5. Complete the timing diagram below. The initial state is 00 and the input sequence is 1 0 1 0 1. You should be able to verify the next state and output using your state diagram/table.



6. What is the output sequence (five values of z) for the input sequence applied above (10101)?

Problem #4.

In this problem you are to design a sequence detector that recognizes the input string 1011. Because you are not asked for a specific implementation, use symbolic states (0, 1, 2, 3, 4, etc.) rather than their binary representations (000, 001, 010, 011, 100, etc.) in the state diagrams and state tables.

1. Construct a state diagram for a Moore machine implementing the sequence detector. Identify both the starting and accepting states.

2. Construct a state table for the Moore machine.

3. Convert the Moore machine state table to an equivalent Mealy machine state table.

4. Can any states in the equivalent Mealy machine be combined? If so, construct the "reduced" state table.

5. Construct the state diagram for the Mealy machine.